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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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22470	7590	06/07/2006	EXAMINER	
HAYNES BEFFEL & WOLFELD LLP P O BOX 366 HALF MOON BAY, CA 94019			PEERS, CHASE W	
			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,766	SUN ET AL.	
Examiner	Art Unit		
Chase Peers	2186		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 17 May 2006.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-15 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-15 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date. ____.
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date. ____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: ____.

The examiner acknowledges the applicant's submission of the amendment dated **4/12/2006**. At this point claims have been amended and claims have been cancelled. Thus, claims are pending in the instant application.

1. TERMINAL DISCLAIMER

One of the Terminal Disclaimers for this application are found to be improper because: 1) the serial number of the application (or number of the patent) which forms the basis for the double patenting rejection is missing or incorrect. 2) 10/699756 is not mentioned in the office action.

2. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

1. Claims 1, 14 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci (Pat No 6792527) and in further in view of Skruhak et al. (Pat No 5412785).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic configured to execute instructions (column 2, lines 5-23 and lines 38-40), a memory adapted to store instructions for a mission function for the integrated circuit, a programmable configuration memory adapted to store the configuration data (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), a processor coupled to memory which executes instructions from memory (column 2, lines 55-64), an interface between

the processor and the configuration memory that supports the initialization function, an interface between the configuration memory and the configurable logic array supporting transfer of configuration data to the configurable logic array, and an interface between the processor and the configurable logic array supporting transfer of configuration data to the configurable logic array (figure 1 and column 2, lines 24-28).

Allegrucci does not explicitly talk about the ability to store instructions for a configuration function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array. However, Skruhak et al. does describe the ability to store instructions for an initialization function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array (column 2 line 30 to column 3 line 3).

Allegrucci and Skruhak et al. are analogous art because they are from a similar problem solving area, responding to initialization events. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the initialization function transfer configuration data to the CLA. The suggestion for doing so would have been to make sure the system is easier to change. Therefore, it would have been obvious to combine Allegrucci and Skruhak et al. for the benefit of simplicity to obtain the invention as specified in claims 1, 14, and 15.

The examiner notes that the CSL cells in the prior art of Allegrucci are configuration points, but are not listed as such. Furthermore, although Elmer et

al. does not expressly disclose the use of a programmable memory adapted to store configuration data, it does disclose the exact same functionality with a second memory area. The examiner also notes that Allegrucci notes that the configurable logic (item 120) is also known as a configurable processor, which means it is capable of executing the code.

2. Claims 2-4 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci and Skruhak et al. as applied to claim 1 above, and further in view of Agrawal (Pat No 6102963).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic configured to execute instructions (column 2, lines 5-23 and lines 38-40), a memory adapted to store instructions for a mission function for the integrated circuit, a programmable configuration memory adapted to store the configuration data (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), a processor coupled to memory which executes instructions from memory (column 2, lines 55-64), an interface between the processor and the configuration memory that supports the initialization function, an interface between the configuration memory and the configurable logic array supporting transfer of configuration data to the configurable logic array, and an interface between the processor and the configurable logic array supporting transfer of configuration data to the configurable logic array (figure 1 and column 2, lines 24-28).

Skruhak et al. describes the ability to store instructions for an initialization function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array (column 2 line 30 to column 3 line 3).

Allegrucci and Skruhak et al. do not disclose expressly having the memory comprises a non-volatile memory store, a floating gate memory store, or a read only memory store.

Agrawal discloses having the memory comprises a non-volatile memory store, a read only memory store (column 2, lines 6-10), or a floating gate memory store (column 10, lines 1-14).

Allegrucci, Skruhak et al. and Agrawal are analogous art because they both regard programmable memory for a system on a chip. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the memory be a non-volatile or floating gate memory. The suggestion for doing so would have been to store data for an extended period of time without worrying about powering the memory. Therefore, it would have been obvious to combine Allegrucci, Skruhak et al. and Agrawal for the benefit of storage to obtain the invention as specified in claims 2-4.

3. Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci and Skruhak et al. as applied to claim 1 above, and further in view of Robb et al. (Pat No 5276839).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic configured to execute instructions (column 2, lines 5-23 and lines 38-40), a memory adapted to store instructions for a mission function for the integrated circuit, a programmable configuration memory adapted to store the configuration data (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), a processor coupled to memory which executes instructions from memory (column 2, lines 55-64), an interface between the processor and the configuration memory that supports the initialization function, an interface between the configuration memory and the configurable logic array supporting transfer of configuration data to the configurable logic array, and an interface between the processor and the configurable logic array supporting transfer of configuration data to the configurable logic array (figure 1 and column 2, lines 24-28).

Skruhak et al. describes the ability to store instructions for an initialization function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array (column 2 line 30 to column 3 line 3).

Allegrucci and Skruhak et al. do not disclose expressly a second store for the mission function.

Robb et al. discloses a second store for the mission function (column 3, lines 43-49).

Allegrucci, Skruhak et al. and Robb et al. are analogous art because they both regard programmable memory for a system on a chip. At the time of the invention it would have been obvious to a person of ordinary skill in the art to store the mission function in memory. The suggestion for doing so would have been for easy access to the function by the processor. Therefore, it would have been obvious to combine Allegrucci, Skruhak et al. and Robb et al. for the benefit of time-saving and easy access to obtain the invention as specified in claim 5.

The examiner notes that although it does not expressly state that the mission function is stored on the memory, it must be noted that for the processor to do its mission for the host system, it must load the mission function and mission data, which would come from the memory.

4. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci and Skruhak et al. as applied to claim 1 above, and further in view of Robb et al. (Pat No 5276839).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic configured to execute instructions (column 2, lines 5-23 and lines 38-40), a memory adapted to store instructions for a mission function for the integrated circuit, a programmable configuration memory adapted to store the configuration data (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), a processor coupled to memory which executes instructions from memory (column 2, lines 55-64), an interface between

the processor and the configuration memory that supports the initialization function, an interface between the configuration memory and the configurable logic array supporting transfer of configuration data to the configurable logic array, and an interface between the processor and the configurable logic array supporting transfer of configuration data to the configurable logic array (figure 1 and column 2, lines 24-28).

Skruhak et al. describes the ability to store instructions for an initialization function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array (column 2 line 30 to column 3 line 3).

Allegrucci and Skruhak et al. do not disclose expressly the memory being a first volatile store for the configuration function and a second store for the mission function.

Robb et al. discloses the memory being RAM (figure 1, item 260) and a second store for the mission function (column 3, lines 43-49).

Allegrucci, Skruhak et al. and Robb et al. are analogous art because they both regard programmable memory for a system on a chip. At the time of the invention it would have been obvious to a person of ordinary skill in the art to store the mission function in memory and to have memory be volatile. The suggestion for doing so would have been for easy access to the function by the processor, low cost, and easily changeable. Therefore, it would have been obvious to combine Allegrucci, Skruhak et al. and Robb et al. for the benefit of

time and cost savings and easy access to obtain the invention as specified in claim 6.

The examiner notes that although it does not expressly state that the mission functions are stored on the memory, it must be noted that for the processor to do its mission for the host system, it must load the mission functions and mission data, which would come from the memory.

5. Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci and Skruhak et al. as applied to claim 1 above, and further in view of Sun et al. (Pat No 6401221).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic configured to execute instructions (column 2, lines 5-23 and lines 38-40), a memory adapted to store instructions for a mission function for the integrated circuit, a programmable configuration memory adapted to store the configuration data (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), a processor coupled to memory which executes instructions from memory (column 2, lines 55-64), an interface between the processor and the configuration memory that supports the initialization function, an interface between the configuration memory and the configurable logic array supporting transfer of configuration data to the configurable logic array, and an interface between the processor and the configurable logic array

supporting transfer of configuration data to the configurable logic array (figure 1 and column 2, lines 24-28).

Skruhak et al. describes the ability to store instructions for an initialization function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array (column 2 line 30 to column 3 line 3).

Allegrucci and Skruhak et al. do not disclose expressly a watchdog timer coupled to the CPU, a configuration function that includes using a timer to generate a reset on a response to an error, upon the initialization event, reexecuting the configuration load and configuration function.

Sun et al. discloses a watchdog timer coupled to the CPU (figure 1, item 122), a configuration function that includes using a timer to generate a reset on a response to an error, upon the initialization event, reexecuting the configuration load and configuration function (column 4, lines 15-19).

Allegrucci, Skruhak et al. and Sun et al. are analogous art because they are from the same field of endeavor, an in circuit programming system that can run downloaded code and reset the system when necessary. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate a watchdog timer and the functions that come with the timer. The suggestion for doing so would have been the ability to reset the system when an error occurs. Therefore, it would have been obvious to combine Allegrucci, Skruhak et al. and Sun et al. for the benefit of resetting the system to obtain the invention as specified in claim 7.

6. Claims 8 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci and Skruhak et al. as applied to claim 1 above, and further in view of Agrawal (Pat No 6102963).

Regarding claim 8, Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic configured to execute instructions (column 2, lines 5-23 and lines 38-40), a memory adapted to store instructions for a mission function for the integrated circuit, a programmable configuration memory adapted to store the configuration data (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), a processor coupled to memory which executes instructions from memory (column 2, lines 55-64), an interface between the processor and the configuration memory that supports the initialization function, an interface between the configuration memory and the configurable logic array supporting transfer of configuration data to the configurable logic array, and an interface between the processor and the configurable logic array supporting transfer of configuration data to the configurable logic array (figure 1 and column 2, lines 24-28).

Skruhak et al. describes the ability to store instructions for an initialization function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array (column 2 line 30 to column 3 line 3).

Allegrucci and Skruhak et al. do not disclose expressly the configuration function including loading the programmable configuration memory via an input port on the integrated circuit.

Agrawal describes the configuration function including loading the programmable configuration memory via an input port on the integrated circuit (column 4, lines 3-14).

Allegrucci, Skruhak et al. and Agrawal are analogous art because they both regard programmable memory for a system on a chip. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the configuration function be loaded via an input port. The suggestion for doing so would have been to protect the configuration function by keeping a master copy at another location. Therefore, it would have been obvious to combine Allegrucci, Skruhak et al. and Agrawal for the benefit of data protection to obtain the invention as specified in claim 8.

Regarding claim 12, Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic configured to execute instructions (column 2, lines 5-23 and lines 38-40), a memory adapted to store instructions for a mission function for the integrated circuit, a programmable configuration memory adapted to store the configuration data (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), a processor coupled to memory which executes instructions from memory (column 2, lines 55-64), an interface

between the processor and the configuration memory that supports the initialization function, an interface between the configuration memory and the configurable logic array supporting transfer of configuration data to the configurable logic array, and an interface between the processor and the configurable logic array supporting transfer of configuration data to the configurable logic array (figure 1 and column 2, lines 24-28).

Skruhak et al. describes the ability to store instructions for an initialization function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array (column 2 line 30 to column 3 line 3).

Allegrucci and Skruhak et al. do not disclose expressly the programmable configuration memory comprising a volatile store.

Agrawal does describe the programmable configuration memory comprising a volatile store (column 3, lines 50-56, and column 6, lines 33-37).

Allegrucci, Skruhak et al. and Agrawal are analogous art because they both regard programmable memory for a system on a chip. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the memory be a volatile memory. The suggestion for doing so would have been to easily change or erase the data on the memory. Therefore, it would have been obvious to combine Allegrucci, Skruhak et al. and Agrawal for the benefit of ease of use to obtain the invention as specified in claim 12.

7. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci and Skruhak et al. as applied to claim 1 above, and further in view of Shukla (Pat No 6345101).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic configured to execute instructions (column 2, lines 5-23 and lines 38-40), a memory adapted to store instructions for a mission function for the integrated circuit, a programmable configuration memory adapted to store the configuration data (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), a processor coupled to memory which executes instructions from memory (column 2, lines 55-64), an interface between the processor and the configuration memory that supports the initialization function, an interface between the configuration memory and the configurable logic array supporting transfer of configuration data to the configurable logic array, and an interface between the processor and the configurable logic array supporting transfer of configuration data to the configurable logic array (figure 1 and column 2, lines 24-28).

Skruhak et al. describes the ability to store instructions for an initialization function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array (column 2 line 30 to column 3 line 3).

Allegrucci and Skruhak et al. do not disclose expressly an initialization function that includes receiving encrypted configuration data via an input port,

decrypting the data and then loading the programmable configuration memory with decrypted configuration data.

Shukla discloses expressly an initialization function that includes receiving encrypted configuration data via an input port, decrypting the data and then loading the programmable configuration memory with decrypted configuration data (column 8, lines 27-47).

Allegrucci, Skruhak et al. and Shukla are analogous art because both deal with downloading data in an encrypted format to a programmable device. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow the initialization function to receive encrypted data, to decrypt it and load it into memory. The suggestion for doing so would have been to increase security. Therefore, it would have been obvious to combine Allegrucci, Skruhak et al. and Shukla for the benefit of security to obtain the invention as specified in claim 9.

8. Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci and Skruhak et al. as applied to claim 1 above, and further in view of Fallon et al. (Pub No 20020191692).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic configured to execute instructions (column 2, lines 5-23 and lines 38-40), a memory adapted to store instructions for a mission function for the integrated circuit, a programmable configuration

memory adapted to store the configuration data (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), a processor coupled to memory which executes instructions from memory (column 2, lines 55-64), an interface between the processor and the configuration memory that supports the initialization function, an interface between the configuration memory and the configurable logic array supporting transfer of configuration data to the configurable logic array, and an interface between the processor and the configurable logic array supporting transfer of configuration data to the configurable logic array (figure 1 and column 2, lines 24-28).

Skruhak et al. describes the ability to store instructions for an initialization function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array (column 2 line 30 to column 3 line 3).

Allegrucci and Skruhak et al. do not disclose expressly an initialization function that includes receiving compressed configuration data via an input port, decompressing the data and then loading the programmable configuration memory with decompressed configuration data.

Fallon et al. discloses expressly an initialization function that includes receiving compressed configuration data via an input port, decompressing the data and then loading the programmable configuration memory with decompressed configuration data (paragraph 69).

Allegrucci, Skruhak et al. and Fallon et al. are analogous art because both deal with downloading data in a compressed format to a programmable device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow the initialization function to receive compressed data, to decrypt it and load it in memory. The suggestion for doing so would have been to increase security. Therefore, it would have been obvious to combine Allegrucci, Skruhak et al. and Fallon et al. for the benefit of security to obtain the invention as specified in claim 10.

9. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci and Skruhak et al. as applied to claim 1 above, and further in view of Lawman (Pat No 6028445).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic configured to execute instructions (column 2, lines 5-23 and lines 38-40), a memory adapted to store instructions for a mission function for the integrated circuit, a programmable configuration memory adapted to store the configuration data (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), a processor coupled to memory which executes instructions from memory (column 2, lines 55-64), an interface between the processor and the configuration memory that supports the initialization function, an interface between the configuration memory and the configurable logic array supporting transfer of configuration data to the configurable logic array, and an interface between the processor and the configurable logic array

supporting transfer of configuration data to the configurable logic array (figure 1 and column 2, lines 24-28).

Skruhak et al. describes the ability to store instructions for an initialization function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array (column 2 line 30 to column 3 line 3).

Allegrucci and Skruhak et al. do not disclose expressly an initialization function that includes receiving compressed configuration data via an input port and then decompressing the data.

Lawman discloses a initialization function that includes receiving compressed configuration data via an input port and then decompressing the data (column 8, lines 12-33).

Allegrucci, Skruhak et al. and Lawman are analogous art because both deal with downloading data in a compressed format to a programmable device. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow the initialization function to receive compressed data and to decompress it. The suggestion for doing so would have been to save time and bandwidth. Therefore, it would have been obvious to combine Allegrucci, Skruhak et al. and Lawman for the benefit of time and bandwidth savings to obtain the invention as specified in claim 11.

10. Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Allegrucci and Skruhak et al. as applied to claim 1 above, and further in view of Trimberger (Pat No 6105105).

Allegrucci discloses an input port which receives data (column 3, lines 36-41), a configuration logic array defined by configuration data stored in configuration points in the configuration logic configured to execute instructions (column 2, lines 5-23 and lines 38-40), a memory adapted to store instructions for a mission function for the integrated circuit, a programmable configuration memory adapted to store the configuration data (column 3, lines 28-41 and column 1 line 66 to column 2 line 4), a processor coupled to memory which executes instructions from memory (column 2, lines 55-64), an interface between the processor and the configuration memory that supports the initialization function, an interface between the configuration memory and the configurable logic array supporting transfer of configuration data to the configurable logic array, and an interface between the processor and the configurable logic array supporting transfer of configuration data to the configurable logic array (figure 1 and column 2, lines 24-28).

Skruhak et al. describes the ability to store instructions for an initialization function used to transfer the configuration data from then configuration memory to the programmable configuration points within the configurable logic array (column 2 line 30 to column 3 line 3).

Allegrucci and Skruhak et al. do not disclose expressly the configuration points comprising either floating gate memory cells, non-volatile charge programmable memory cells, or non-volatile programmable memory cells.

Trimberger discloses the configuration points comprising either floating gate memory cells, non-volatile charge programmable memory cells, or non-volatile programmable memory cells (column 4, lines 12-21).

Allegrucci, Skruhak et al. and Trimberger are analogous art because they are both processing systems that employ reconfigurable programmable logic. At the time of the invention it would have been obvious to a person of ordinary skill in the art to make the configuration points comprise floating gate or non-volatile memory cells. The suggestion for doing so would have been to make sure the data can survive a loss of power or reset to the system. Therefore, it would have been obvious to combine Allegrucci, Skruhak et al. and Trimberger for the benefit of not losing data to obtain the invention as specified in claim 13.

3. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

Applicant's arguments filed 4/12/2006 have been fully considered but they are not deemed to be persuasive and, as required by M.P.E.P. § 707.07(f), a response to these arguments appears below.

a. ARGUMENTS CONCERNING FORMAL MATTERS

The applicant's traversal of the formal requirements requested by the examiner are addressed in the following section as required by M.P.E.P. §

707.07(f).

4. ARGUMENTS CONCERNING PRIOR ART REJECTIONS

1st POINT OF ARGUMENT:

Regarding all remarks, as per the terminal disclaimer, new rejections have been made and all further arguments are now moot.

5. CLOSING COMMENTS

Conclusion

6. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. § 707.07(i):

a(1) SUBJECT MATTER CONSIDERED ALLOWABLE

No subject matter was considered allowable.

a(2) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, all claims have received a second action on the merits and are subject of a second action non-final.

For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

7. DIRECTION OF ALL FUTURE REMARKS

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chase Peers whose telephone number is

(571) 272-6757. The examiner can normally be reached on from Monday to Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


PIERRE BATAILLE
PRIMARY EXAMINER
5/23/06